

Pentium Pro and Pentium II System Architecture (2nd Edition)

By MindShare Inc., Tom Shanley



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Pentium Pro and Pentium II System Architecture is a book for anyone doing hardware design or support, as well as to any developers who write low-level system code.

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Pentium Pro and Pentium II System Architecture (2nd Edition) By MindShare Inc., Tom Shanley Bibliography

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Editorial Review

From the Inside Flap

The MindShare Architecture Series

The MindShare Architecture book series includes: ISA System Architecture, EISA System Architecture, 80486 System Architecture, PCI System Architecture, Pentium System Architecture, PCMCIA System Architecture, PowerPC System Architecture, Plug-and-Play System Architecture, CardBus System Architecture, Protected Mode Software Architecture, USB System Architecture, Pentium Pro and Pentium II System Architecture, and FireWire System Architecture: IEEE 1394. The book series is published by Addison-Wesley.

Rather than duplicating common information in each book, the series uses the building-block approach. ISA System Architecture is the core book upon which most of the others build. The figure below illustrates the relationship of the books to each other.

Cautionary Note

The reader should keep in mind that MindShare's book series often deals with rapidly-evolving technologies. This being the case, it should be recognized that each book is a "snapshot" of the state of the targeted technology at the time that the book was completed. We attempt to update each book on a timely basis to reflect changes in the targeted technology, but, due to various factors (waiting for the next version of the spec to be "frozen," the time necessary to make the changes, and the time to produce the books and get them out to the distribution channels), there will always be a delay.

What This Book Covers

The purpose of this book is to provide a detailed description of the Pentium Pro and Pentium II processors both from the hardware and the software perspectives. As with our other x86 processor books, this book builds upon and does not duplicate information provided in our books on the previous generation processors. As an example, our Pentium Processor System Architecture book provided a detailed description of the APIC module, while this book only describes differences between the two implementations.

What this Book Does not Cover

This book does not describe the x86 instruction repertoire. There are a host of books on the market that already provide this information. It does, however, describe the new instructions added to the instruction set.

Organization of This Book

Pentium Pro and Pentium II System Architecture extends MindShare's coverage of x86 processor architecture to the Pentium Pro and Pentium II processors. The author considers this book to be a companion to the MindShare books entitled 80486 System Architecture, Pentium Processor System Architecture, and Protected Mode Software Architecture (all published by Addison-Wesley). The book is organized as follows: Part 1: System Overview Chapter 1: System Overview Part 2: Processor's Hardware Characteristics Hardware Section 1: The Processor Chapter 2: Processor Overview Chapter 3: Processor Power-On

Configuration Chapter 4: Processor Startup Chapter 5: The Fetch, Decode, Execute Engine Chapter 6: Rules of Conduct Hardware Section 2: Bus Intro and Arbitration Chapter 8: Bus Electrical Characteristics Chapter 9: Bus Basics Chapter 10: Obtaining Bus Ownership Hardware Section 3: The Transaction Phases Chapter 11: The Request and Error Phases Chapter 12: The Snoop Phase Chapter 13: The Response and Data Phases Hardware Section 4: Other Bus Topics Chapter 14: Transaction Deferral Chapter 15: IO Transactions Chapter 16: Central Agent Transactions Chapter 17: Other Signals Part 3: Pentium II Processor Chapter 18: Pentium II Processor Part 4: Processor's Software Characteristics Chapter 19: Instruction Set Enhancements Chapter 20: Register Set Enhancements Chapter 21: BIOS Update Feature Chapter 22: Paging Enhancements Chapter 23: Interrupt Enhancements Chapter 24: Machine Check Architecture Chapter 25: Performance Monitoring and Timestamp Chapter 26: MMX: Matrix Math Extensions Part 5: Overview of Intel Pentium Pro Chipsets Chapter 27: 450GX and KX Chipsets Chapter 28: 440FX Chipset

Who this Book is For

This book is intended for use by hardware and software design and support personnel. Due to the clear, concise explanatory methods used to describe each subject, personnel outside of the design field may also find the text useful.

Prerequisite Knowledge

It is highly recommended that the reader have a good knowledge of x86 processor architecture. Detailed descriptions of the 286 and 386 processors can be found in the MindShare book entitled ISA System Architecture. Detailed descriptions of the 486 and Pentium processors can be found in the MindShare books entitled 80486 System Architecture and Pentium Processor System Architecture, respectively. Detailed descriptions of both real and protected mode operation can be found in the MindShare book entitled Protected Mode Software Architecture. All of these books are published by Addison-Wesley.

Documentation Conventions

This document utilizes the following documentation conventions for numeric values.

Hexadecimal Notation

All hex numbers are followed by an "h." Examples:

9A4Eh 0100h

Binary Notation

All binary numbers are followed by a "b." Examples:

0001 0101b 01b

Decimal Notation

Numbers without any suffix are decimal. When required for clarity, decimal numbers are followed by a "d." The following examples each represent a decimal number:

16

255

128d

Signal Name Representation

Each signal that assumes the logic low state when asserted is followed by a pound sign (#). As an example, the HITM# signal is asserted low when a snoop agent has a hit on a modified line in its caches.

Signals that are not followed by a pound sign are asserted when they assume the logic high state.

Warning

The majority of the processor's signal pins are active low signals (e.g., all of the pins involved in a transaction). All tables in the Intel Pentium Pro Volume One data book, however, represent an asserted signal (in other words, in the electrically low state) with a one, while deasserted signals (electrically high) are represented by a zero in table entries. In other words, a "logical" one in a table indicates that the respective signal pin is asserted (in the electrically low state).

As an example, when a table entry indicates a one for the HITM# signal state, this indicates that it is asserted (electrically low).

Identification of Bit Fields (logical groups of bits or signals)

All bit fields are designated in little-endian bit ordering as follows:

X:Y,

where "X" is the most-significant bit and "Y" is the least-significant bit of the field. As an example, the IOPL field in the EFLAGS register consists of bits 13:12, where bit 13 is the most-significant and bit 12 the least-significant bit of the field.

Register Field References

Bit fields in registers are frequently referred to using the form Regfield name. As an example, the reference CR4DE refers to the Debug Extensions bit in Control Register 4.

Resources

The Intel Developers' web site contains many documents available for download that provide excellent reference materials. We have a hot-link to their web site on our web site (see next section).

Visit Our Web Site

Our Web site contains a listing of all of our courses and books. In addition, it contains errata for a number of the books, a hot link to our publisher's web site, course outlines, and hot links to other useful web sites.

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From the Back Cover

"This series of books is truly an important part of my library. ... I would recommend them to anyone doing hardware design or support, as well as to any developers who write low-level system code." -Paula Tomlinson, Windows Developer's Journal

Pentiumi Pro and Pentiumi II System Architecture, Second Edition, details the internal architecture of these two processors, describing their hardware and software characteristics, the bus protocol they use to communicate with the system, and the overall machine architecture. It also describes the BIOS Update Feature.

Written for computer hardware and software engineers, this book offers insight into how the Pentium Pro and Pentium II family of processors translates legacy x86 code into RISC instructions, executes them out-of-order, and then reassembles the result to match the original program flow. In detailing the Pentium Pro and Pentium II processors' internal operations, the book reveals why the processors generate various transaction types and how they monitor bus traffic generated by other entities to ensure cache consistency.

This new edition includes comprehensive coverage of the Pentium II processor. It highlights the differences between the Pentium Pro and Pentium II processors, in particular, the Slot 1 connector and the processor cartridge design utilized by the Pentium II and intended for use in future Intel processors. It features the Pentium II's support for the MMX instruction set and registers, and shows how it is optimized for 16-bit code execution. This book also describes the Pentium II's L2 cache and its support for power-conservation modes.

Pentiumi Pro and Pentiumi II System Architecture, Second Edition, also covers:

- the relationship of Pentium Pro and Pentium II processors to other processors, PCI bridges, caches, and memory
- detailed descriptions of the data, code, and L2 caches
- power-on configuration and processor startup
- transaction deferral
- instruction, register set, paging, and interrupt enhancements to the Pentium Pro and Pentium II

- BIOS Update Feature
- Machine Check Architecture
- performance monitoring and the Time Stamp Counter
- MMX register and instruction set supported by the Pentium II
- overview of the Intel 450KX, 450GX, and 440FX chipsets

The PC System Architecture Series is a crisply written and comprehensive set of guides to the most important PC hardware standards. Each title is designed to illustrate the relationship between the software and hardware and explains thoroughly the architecture, features, and operations of systems built using one particular type of chip or hardware specification.

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About the Author

MindShare, Inc. is one of the leading technical training companies in the hardware industry, providing innovative courses for dozens of companies, including Intel, IBM, and Compaq.

Tom Shanley, president of MindShare, Inc., is one of the world's foremost authorities on computer system architecture. In the course of his career, he has trained thousands of engineers in hardware and software design.

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Users Review

From reader reviews:

Randy Johnson:

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Patricia French:

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