



Electronic Design Automation: Synthesis, Verification, and Test (Systems on Silicon)

From Brand: Morgan Kaufmann

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This book provides broad and comprehensive coverage of the entire EDA flow. EDA/VLSI practitioners and researchers in need of fluency in an "adjacent" field will find this an invaluable reference to the basic EDA concepts, principles, data structures, algorithms, and architectures for the design, verification, and test of VLSI circuits. Anyone who needs to learn the concepts, principles, data structures, algorithms, and architectures of the EDA flow will benefit from this book.

- Covers complete spectrum of the EDA flow, from ESL design modeling to logic/test synthesis, verification, physical design, and test - helps EDA newcomers to get "up-and-running" quickly
- Includes comprehensive coverage of EDA concepts, principles, data structures, algorithms, and architectures - helps all readers improve their VLSI design competence
- Contains latest advancements not yet available in other books, including Test compression, ESL design modeling, large-scale floorplanning, placement, routing, synthesis of clock and power/ground networks - helps readers to design/develop testable chips or products
- Includes industry best-practices wherever appropriate in most chapters - helps readers avoid costly mistakes

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Editorial Review

From the Back Cover

As semiconductor applications continue to advance and proliferate, the industry is increasingly dependent on design technologies for design closure and for meeting productivity goals. Electronic design automation (EDA), which has driven advances in design technologies for the past 30 years, will continue to play a critical role in the semiconductor food chain.

This book brings together a set of core EDA topics which provides an essential, fundamental understanding of the EDA tasks and the design process. Collectively, these topics cover the core knowledge, software tools, algorithms, methodologies, and infrastructure required to optimize synthesis, verification, and manufacturing test of a functional and reliable integrated circuit.

The contents found within this book will enable the reader to understand fundamental EDA algorithms for synthesis and verification as well as very-large-scale integration (VLSI) test principles and DFT architectures to tackle EDA and test problems as advances in technology enter the nanometer era.

About the Author

Laung-Terng Wang, Ph.D., is founder, chairman, and chief executive officer of SynTest Technologies, CA. He received his EE Ph.D. degree from Stanford University. A Fellow of the IEEE, he holds 18 U.S. Patents and 12 European Patents, and has co-authored/co-edited two internationally used DFT textbooks- VLSI Test Principles and Architectures (2006) and System-on-Chip Test Architectures (2007).

Yao-Wen Chang, Ph.D., is a Professor in the Department of Electrical Engineering, National Taiwan University. He received his Ph.D. degree in Computer Science from the University of Texas at Austin. He has published over 200 technical papers, co-authored one book, and is a winner of the ACM ISPD Placement (2006) and Global Routing (2008) contests.

Kwang-Ting (Tim) Cheng, Ph.D., is a Professor and Chair of the Electrical and Computer Engineering Department at the University of California, Berkeley. A Fellow of the IEEE, he has published over 300 technical papers, co-authored three books, and holds 11 U.S. Patents.

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Christi Shoup:

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